REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application, and for withdrawing the previous rejection. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 13, 18, 23, 27, 32 and 36. The arguments supporting patentability of the claims are provided below.

I. The Claims

The present invention, as recited in independent device Claim 10, for example, is directed to a dynamically reconfigurable processing unit comprising a microprocessor, and an embedded Flash memory for non-volatile storage of code, data and bit-streams. The embedded Flash memory comprises a field programmable gate array (FPGA) port. The dynamically reconfigurable processing unit further comprises a direct memory access (DMA) channel, and an S-RAM embedded FPGA for FPGA reconfigurations. The S-RAM embedded FPGA comprises an FPGA programming interface connected to the FPGA port of the embedded Flash memory through the DMA channel. The microprocessor, the embedded Flash memory, the DMA channel and the S-RAM embedded FPGA are integrated as a single chip.

The embedded S-RAM FPGA can thus be reconfigured so that the processing unit is dynamically reconfigurable. The dynamically reconfigurable processing unit advantageously supports application-dependent configurations. The embedded

Flash memory advantageously provides bit-streams from its FPGA port to the FPGA programming interface via the DMA channel so that the S-RAM embedded FPGA can be reconfigured. The DMA channel advantageously speed-ups downloading of the bit-streams to the FPGA programming interface.

Independent device Claim 19 is also directed to a reconfigurable processing unit comprising a microprocessor, a system bus connected to the microprocessor, and an embedded Flash memory comprising a code port and a data port connected to the system bus for interfacing with the microprocessor. The Flash memory also comprises a field programmable gate array (FPGA) port. A direct memory access (DMA) channel is connected to the system bus and to the FPGA port of the embedded Flash memory. An embedded FPGA is for FPGA reconfigurations and comprises a FPGA programming interface connected to the DMA channel for interfacing with the FPGA port of the Flash memory.

Independent method Claim 28 is directed to a method for making a reconfigurable processing unit as defined in independent device Claim 10.

II. The Claims Are Patentable

Independent Claims 10, 19 and 28 were rejected over the Iwata et al. patent in view of the Bocchi patent. The Examiner cited the Iwata et al. patent as disclosing a processing unit **1** in FIG. 1 as comprising a microprocessor **3**, an embedded Flash memory **5** comprising a port, a direct memory access (DMA) channel **7**, and an embedded SRAM **6**.

As correctly noted by the Examiner, the Iwata et al. patent fails to disclose that the embedded SRAM **6** is connected to the port of the embedded Flash memory **5** via the DMA channel **7**. The Examiner cited the Bocchi patent as disclosing in FIG. 1 a Flash memory **62** comprising a port connected to a FPGA **64**, and an SRAM **68** comprising a FPGA programming interface (**CPLD**) connected to a FPGA port of the Flash memory **62**.

The Examiner has taken the position that it would have been obvious to one skilled in the art at the time of the invention to modify Iwata et al. to incorporate the functionality of the FPGA programming interface (**CPLD**). The Examiner further characterized the **CPLD** as operating as a DMA channel for interfacing with the SRAM **68**.

The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. The embedded Flash memory **5** in the Iwata et al. patent is part of a debugging operation. Reference is directed to column 5, lines 11-14 of Iwata et al., which provides:

> "The OR circuit **5b** and the flash internal control circuit **5c** make up a means that permits a rewrite of the internal flash-memory **5** at the debug mode without distinction of the input value of a FP terminal 5a." (Emphasis added).

Moreover, the Iwata et al. patent fails to disclose that the SRAM **6** is an SRAM embedded FPGA for FPGA

reconfigurations as in the claimed invention. In fact, since the Iwata et al. is directed to debugging of the embedded Flash memory **5**, there is no mention of reprogramming the SRAM **6**.

In the Bocchi patent, the CPLD **60** is a complex programmable logic device for controlling multiple motors, and the CPLD **60** is separate from the FPGA **64**. The FPGA **64** is programmed via the Flash memory **62** and not the CPLD **60**. Reference is directed to column 5, lines 5-14 of Bocchi, which provides:

> "For the controller **10** to function correctly after power-on or reset, additional steps must be completed after programming the CPLD **60**. Valid programs must be downloaded from the application program into the flash memory **62**. Code for the field-programmable gate array (FPGA) **64** and the embedded code for the central processing unit (CPU) **66** is downloaded into the flash memory **62** through a flash programming port (not shown), which is a parallel interface to the CPLD **60**." (Emphasis added).

The Bocchi patent thus fails to disclose that the CPLD **60** is used to program the FPGA **64**. Instead, the FPGA **64** is programmed via the Flash memory **62**. Accordingly, it is submitted that independent Claim 10 is patentable over the Iwata et al. patent in view of the Bocchi patent.

Independent Claims 19 and 28 are similar to independent Claim 10. Therefore, it is submitted that these claims are also patentable over the Iwata et al. patent in view of the Bocchi patent. In view of the patentability of independent Claims 10,

19 and 28, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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